REMARKS

Applicants appreciate the thorough examination of the present application as evidenced by the Action. However, Applicants request withdrawal of the objections and rejections for at least the reasons discussed below.

The Objection to the Specification:

The abstract is objected to as exceeding 150 words in length. Office Action, p. 2. The abstract has been amended above to reduce the word count to under 150 words. Accordingly, the objection to the abstract should be withdrawn as obviated.

The Section 112 Rejections:

Claims 1-12 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. Office Action, p. 2. In particular, Claims 1 and 4 are rejected for lack of antecedent basis for the "first" sub logic circuit unit. Office Action, p. 3. Claims 1 and 4 have been amended above to replace "first" with "input side." Accordingly, Applicants request withdrawal of this rejection as obviated.

Claims 1 and 4 also stand rejected as "narrative and indefinite" based on various recitations in the claims and an assertion that the claims "are replete with grammatical and idiomatic errors." Office Action, p. 3. Applicants respectfully disagree. As an initial matter, other than general allegations and extensive excerpts of claim language, these rejections fail to explain what is not clear. Applicants submit that the claims are definite and fully supported by both the present specification and the Korean priority application. These claims fully meet the criteria provided under 35 U.S.C. § 112 and the Office Action fails to assert any basis to support the alleged indefiniteness of these claims. Accordingly, at least as the Office Action fails to cite a basis for the rejections, these Section 112 rejections should be withdrawn.

To assist the Examiner in considering these claims, Applicants provide the following re-casting of **previously pending** Claim 1 with numbers added adjacent various of the recitations. These numbers are provided solely by way of example to assist

the Examiner in understanding the grammar and idiom of the claims and are not to be construed as limiting the scope of the claims to the identified illustrated embodiments.

An integrated circuit device comprising:

a core block **530** configured for dynamic simulation testing and having an associated plurality of output ports **(connecting 530 to 540 and carrying data C2Di)**, wherein the core block generates core output data for the plurality of ports responsive to output data for the plurality of output ports input to a plurality of input ports **(connections from 520 to 530)** of the core block;

an input side sub logic circuit unit **510** configured for dynamic simulation testing and coupled to the input ports of the core block **530** that generates sub data **(carried on connections from 510 to 520)** for the plurality of input ports **(connections from 520 to 530)** responsive to data input **MDI** to the input side sub logic circuit unit **510**; and

a multiplexer (MUX) unit **520** between the core block **530** and the input side sub logic circuit unit **510** that selectively provides the sub data **(carried on connections from 510 to 520)** or the output data **C2Di** as inputs **(carried on connections from 520 to 530)** to the input ports of the core block responsive to a MUX control signal **TI**.

Similarly for **previously pending** Claim 4:

An integrated circuit device comprising:

a core block **530** having a plurality of output ports **(connecting 530 to 540)** and a plurality of input ports **(connecting 520 to 530)** and a vector input terminal **(carrying data TDI)**, wherein the core block generates core internal data **C1D1i** responsive to output data **(carried on connections from 520 to 530)** from the input ports and wherein the core block is configured to output the core internal data **C1D1i** during scan testing and to selectively generate core output data **C2D1i** for the output ports **(connecting 530 to 540)** responsive to the core internal data **C1D1i** or to test vector serial input data **TDI** from the vector input terminal;

an input side sub logic circuit unit **510** configured for dynamic simulation testing and coupled to the input ports of the core block that generates sub data **(carried on connections from 510 to 520)** for the plurality of input ports **(connecting 520 to 530)** responsive to data input **MDI** to the input side sub logic circuit unit; and

a multiplexer (MUX) unit **520** between the core block and the input side sub logic circuit unit that selectively provides the sub data **(carried on connections from 510 to 520)** or the output data **C2DNi** as inputs to the input ports **(connecting 520 to 530)** of the core block responsive to a MUX control signal **TI**.

Furthermore, while Applicants believe the Section 112 rejections were unfounded

for the reasons discussed above, additional stylistic changes have been made to Claims 1 and 4 above. However, it is to be understood that, as illustrated by the example reference numbers show above, these changes do not affect the scope of these claims. Thus, these amendments are merely presented to expedite consideration of the present application by the Examiner.

The Section 102 Rejections:

Claims 1-24 stand rejected under 35 U.S.C. § 102(e) as anticipated by United States Patent No. 6,877,122 to Whetsel ("Whetsel"). Office Action, p. 4. In particular, with respect to independent Claims 1, 13, 15 and 20, the Office Action asserts, among other things, that the input linking circuit 602 of Whetsel discloses the input side sub logic circuit unit and the multiplexers 608-610 of Whetsel disclose the MUX. Even assuming this application of Whetsel is correct, the multiplexers 608 to 610 are the input linking circuitry 602 as seen in Figure 6B of Whetsel. However, as recited in Claim 1, the MUX unit is "between the core block and the input side sub logic circuit unit." Thus, the rejection of Claim 1 should be withdrawn for at least these reasons as the multiplexers of Whetsel are the alleged input side sub logic circuit unit and cannot reside between themselves and the cores 1-3.

In addition, the rejection asserts, without basis, that the various circuits of Whetsel cited in the rejection are "configured for dynamic simulation testing." Office Action, p. 4. However, in searching the USPTO online patent database, Applicants' undersigned representative can find no reference to "dynamic simulation testing" or even to "simulation" anywhere in Whetsel. Accordingly, Applicants submit that the rejection of Claim 1 should also be withdrawn for at least these additional reasons.

Independent Claims 13, 15 and 20 are also patentable at least for substantially similar reasons based on corresponding recitations therein. In addition, the claims depending on independent Claims 1, 13, 15 and 20 are patentable at least based on their dependence from these patentable independent claims.

Independent Claims 4, 14, 16 and 21 are patentable for similar reasons to Claim 1

as they each include recitations related to dynamic simulation testing and a MUX unit separate from a core block and a sub logic circuit unit. Accordingly, they are patentable at least for substantially similar reasons to those discussed above with reference to Claim 1.

In addition, these claims include various recitations related to scan testing and/or vector input terminals. While Whetsel does discuss scan operations, Applicants submit the rejections fail to apply Whetsel to the particular related recitations of each of these independent claims in a manner establishing even a prima facia case of anticipation. For example, with reference to Figure 6A of Whetsel, the cores 1-3 appear to each only include one data input SI and one output SO. The remaining signals appear to be control signals. Accordingly, with reference, for example, to Claim 4, it is unclear what the rejection alleges would be the respective output ports, input ports **and** vector input terminal of the core block. If SO are output ports and SI are input ports as asserted, there simply is no vector input terminal. Applicants' undersigned representative can find no reference to the vector input terminal in the Office Action rejections of Claims 4, 14, 16 and 21. Various other recitations of ones of these claims and the relationship between such recitations are similarly overlooked in the anticipation rejections. Accordingly, the rejections of Claims 4, 14, 16 and 21 as anticipated should also be withdrawn for at least these additional reasons.

In light of the lack of clarity of the basis of the rejections of the independent claims, Applicants will not attempt to address separate patentability grounds of the dependent claims at this time. However, if the Examiner should continue to retain the rejections over Whetsel after reviewing Applicants' explanatory comments above and arguments regarding the deficiencies of the rejections, Applicants request clarification of the basis of the rejections by clearer indications of the alleged correspondence between Whetsel and each of the recitations of the respective claims so that Applicants can respond more fully.

CONCLUSION

Applicants respectfully submit that the references cited in the present rejections do not disclose or suggest the present invention as claimed. Accordingly, Applicants respectfully request reconsideration of the rejections by the Examiner and allowance of all the pending claims and passing this application to issue.

Respectfully submitted,

Robert W. Glatz
Registration No. 36,811

Myers Bigel Sibley & Sajovec
P.O. Box 37428
Raleigh, NC 27627
(919) 854-1400 phone
(919) 854-1401 fax

Certificate of Mailing under 37 CFR 1.8

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on May 9, 2006.

Carey Gregory
491886